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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,742	05/08/2006	Toshio Sunaga	JP920030200US1	4737

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

MAIL DATE	DELIVERY MODE
03/17/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,742	SUNAGA ET AL.	
	Examiner	Art Unit	
	LY D. PHAM	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/16/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 12/18/2008 has been entered. Claims 1, 3, and 4 have been amended.

2. Claims 1 – 6 are pending.

Response to Arguments

3. Applicant's arguments filed 12/18/2008 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "*applicant's latches PFPLL are separate elements and are coupled between buffer circuits (WB) and the secondary sense amplifiers,…*") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In other words, though it is recognized that the claimed latches are part of the memory apparatus including the buffer circuits, and the latches are not the buffer circuits, the instant buffer circuits (and how they technically connect to the other elements in the claim) must be expressly claimed/set forth as a separate component in order for the latches to be recognized differently. As the claims stand, the latch circuits

in Fujisawa were applied simply for the purpose of matching the claimed limitations, which, as far as what is claimed in the claims, the "elements" taught in Fujisawa satisfies the invention sought to be protected.

The foregoing establishes ground for the rejection which follows.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujisawa et al. (US Pat Pub 2004/0004890).

Regarding **claims 1 and 4**, Fujisawa et al. discloses a semiconductor memory and its corresponding burst operation method (figs. 1 – 11) for the semiconductor memory having data I/O buses (referred to as I/O lines, paragraphs 0003, 0005 – 0008, 0041, etc…), a plurality of latch circuits connected in common to each of said data I/O buses (referred to as buffer circuits, paragraphs 0046, 0055, 0070, 0087, 0114, 0118, 0119), and a memory cell array (fig. 1, 2), in which said memory cell array includes a plurality of bi line pairs (paragraphs 0059, 0071, see also fig. 6B), a plurality of bit switches (referred to as column select switches activated by column select lines YS#, paragraph 0059) connected between said plurality of latch circuits and said plurality of bit line pairs and divided into a plurality of groups (referred to as two sub blocks 0 and 1

for each of the four banks, fig. 2A), a plurality of column selection lines (YS# indicated above) provided so as to correspond to said plurality of groups and each of which is connected to a plurality of bit switches included in the corresponding group, and a plurality of sense amplifiers (paragraph 0042, 0044 – 0046, 0048, 0058 – 0118) connected to said plurality of bit line pairs, the burst operation method comprising the steps of:

activating said sense amplifiers (paragraph 0026, 0048, claim text 15); and

driving two or more of said column selection lines in order during activation of said sense amplifers (paragraphs 0026, 0048, wherein eight sense amplifiers are activated simultaneously with activation of 4 column selector lines).

As per **claims 2 and 5**, the step of selecting the block is considered inherent as it must be the case before the respective sense amplifiers are activated with the corresponding block columns, which are simultaneously activated.

As per **claims 3 and 6**, Fujisawa et al. also disclose the semiconductor memory operates in synchronization with an external clock (paragraph 0049, 0070); and

said two or more of the column selection lines are driven in order synchronously with the external clock in said column selection line driving step (paragraph 0070, "... data synchronizes with the front edge of a clock...", and also paragraph 0073).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See references additionally cited for features and disclosures considered relevant to the claimed invention.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LY D. PHAM whose telephone number is (571)272-1793. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ly D Pham/
Primary Examiner, Art Unit 2827
March 13, 2009